National Aeronautics and Space Administration

FY11 End of Year Report for NEPP DDR2 Reliability

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NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

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TABLE OF CONTENTS

ABSTRACT

This document reports the status of the NASA Electronic Parts and Packaging (NEPP) Double Data Rate 2 (DDR2) Reliability effort for FY2011. This year's work concentrated on a 1000-hour life test of DDR2 devices, development of resources to enable additional test methods, and review of the reliability measurements appropriate to NASA programs interested in using DDR2 devices.

1000-hour test data on 78-nm, 2-Gb DDR2 SDRAMs from Micron and Samsung are presented as part of an ongoing effort to research mechanisms for reliability and physics of failure in order to support general scaled Complementary Metal-Oxide Semiconductor (CMOS) reliability.

The commercial field programmable gate array (FPGA) board based test system capable of parallel operation of up to nine devices developed in FY2010 was used to collect device-under-test (DUT) data. This system collects parametric data correlated with operating mode and data retention characteristics of the storage cells. This system has been used to collect data on devices at elevated voltage and elevated temperature. In addition, alternate test apparatuses have been evaluated for potential benefit to the overall NEPP DDR2 efforts, including synergistic work with other centers.

This year's test results and further examination of appropriate test conditions and technologies revealed key elements required for the future direction of this task. First, testing of technology-driven parameters is of limited value due to extensive manufacturer efforts to control the technology. Second, testing focused on determining the reliability of individual devices provides value that the manufacturer cannot provide, including pattern sensitivity, flight-like operation, data imprinting, and examination of bit quality. Third, key operational conditions relevant to NASA may be outside the normal operating parameters of devices, resulting in alternative parameters for use. Finally, fourth, it was determined that obtaining test devices mounted to DIMMs will enable rapid procurement of test devices and keep the test system and DUTs interchangeable with test equipment from other groups.

1.0 CONTEXT AND INTRODUCTION

The NEPP DDR2 Devices task for FY11 continued expansion of test capability for DDR2 devices against reliability parameters. Work included hardware, software, and firmware development, test operations on 78-nm DDR2 devices, and research and collaboration relevant to test methods and test devices.

Work this year included continuation of test operations from FY10 characterizing the device operating current and cell data retention characteristics as a function of exposure to stress environments [1]. The test approach was to expose DDR2 devices to voltage and temperature stress environments up to 125°C and 2.7 V for 1000 hours. The test devices were characterized to observe changes in cell retention as a function of this stress, along the lines of earlier work on test structures as in [2].

78-nm, 2-Gb DDR2 devices from Micron and Samsung were the sample test devices. These devices were a slightly older generation than desired. However, because they are larger feature size they more close match earlier test devices.

DDR2 devices play an important role in upcoming mission opportunities for NASA. These devices are the memory of choice for supporting modern microprocessors (in addition to DDR3). Computer and buffer applications of DDR2 are likely to emerge in the next few years if they are not already in the works. Thus, knowledge of appropriate methods to perform reliability testing of DDR2 devices is increasingly important.

This NEPP task seeks to enable viable reliability testing of DDR2 devices through hardware and software development. This will enable operation and examination of likely NASA uses. The results of this work will help to establish viable test protocols for use on potential flight parts.

The reader is encouraged to refer to the FY11 DDR2 test report "Interim Test Status Report for NEPP Scaled CMOS" [3].

1.1 FY10 Summary

For FY10, work primarily followed three thrusts. The first was development of the DDR2 Reliability Tester (D2RT). The second was establishing a viable test approach to determine reliability test methods targeted at identifying technology qualification methods for arbitrary DDR2 devices. The third thrust was performing reliability testing on 78-nm SDRAMs selected for application of the selected test methods.

1.1.1 D2RT Development

D2RT development included the following key points. We established a viable hardware approach taking into account the desire to keep the test system inexpensive to scale. The system is capable of operating DUTs through modified environmental chambers. And the logic and software designs approaches are modular and easy to migrate. The hardware approach is shown schematically in **Figure 1-1**.

This system includes several design breakpoints where additional resources could be interconnected. The computer is a basic laptop running Visual C++ 2008 or later. The computer can include connections to multiple USB interfaces based on the Opal Kelly 3001 or 3005 units. In the case of the Opal Kelly 3005, up to three FPGA eval board connectors can be used simultaneously. Additionally, the FPGA eval boards are symmetric up to the Mezzanine card which defines the interface to the DUT.

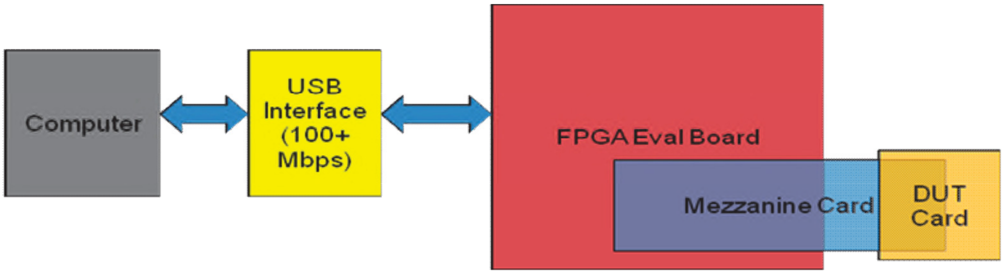

Figure 1-1. Basic test system structure for the DDR2 Reliability Tester (D2RT).

For FY11 we were able to demonstrate operation of up to three FPGA eval boards on a single laptop. We were also able to demonstrate reliable operation of the single-DUT port "mezzanine card A" (MCA), and the Samsung and Micron DDR2 test devices.

1.1.2 Test Methods

Due to findings of the earlier Scaled CMOS NEPP task it was apparent that significant cell degradation would be observed with stress exposure [2]. Because of this we chose to measure cell retention as a first effort in identifying technology degradation, with the intention of building a more complete technology examination approach by building a library of techniques to observe technology parameters. It should be noted that during this year the test results were not consistent with earlier findings regarding technology degradation and there are a few possible explanations for this.

The most viable explanation of differences between earlier work and the findings discussed in this report is that previous testing was performed on test structures where technology degradation could be directly observed while here we were testing packaged parts that included internal mechanisms to protect against voltage acceleration and may also have included mechanisms to limit effects from temperature or even to protect against degraded cell performance, making accurate measurements very difficult. However, there are some clear discrepancies that may not be explained by this argument.

1.1.3 Reliability Testing

Reliability testing of 78-nm DDR2 was started under this task in FY10, and is reported in more detail for FY11 in Section 4.0. The initial results include only the pre-stress characterization and some initial findings regarding characterization curves as a function of stress time. **Figure 1-2** below shows a prestress retention curve compared to another curve taken at 245 hours of stress at 125ºC and 2.7 V.

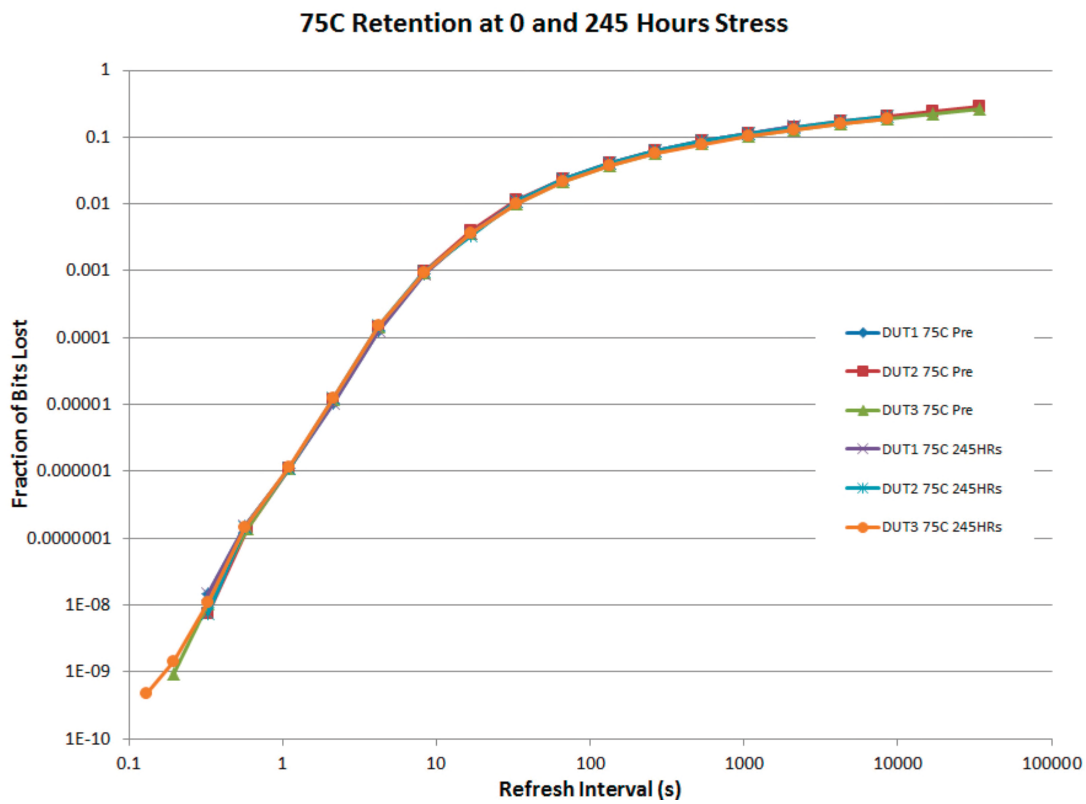

Figure 1-2. Example of pre-stress and 245-hour retention curves taken for 78-nm DDR2 devices from Samsung for FY10.

2.0 TEST PARTS

Test devices continue to be a major concern for the NEPP DDR2 Devices task due to part procurement and preparation for test. This problem was discussed this year with other aerospace industry DDR2 test groups. We found that the most effective way to obtain test devices is to buy unbufferred DDR2 DIMMs (dual inline memory modules).

In this section we discuss all test devices relevant to this work. We start with the test devices desired for testing, then we cover those being used for FY11 stress testing, and, finally, we present details about DDR2 DIMMs for use in future testing.

2.1 Test Part Requirements

For this NEPP program we desire to examine parts with potential application in NASA missions, and also those that are likely to be applicable into the future. Because of the inherent latency involved in part procurement for missions, it is likely that DDR2 devices purchased for flight will be those that are or were mass-produced recently. Current DRAM devices are being produced in 50-nm and smaller feature size.

The test devices which were used to develop the FY10 test approach were 78 nm. These devices are simply too old and too large in feature size to be relevant for future testing.

Previous part-by-part testing required test parts that cost approximately $150/DUT. Testing was limited to only three devices per test point. We believe a statistically significant sample for reliability testing needs to include more test parts, and the cost per DUT must be reduced as much as possible.

2.2 Test Devices for FY11 Stress Testing

For FY11 testing was performed on 78-nm DDR2 SDRAMs from Samsung and Micron [4,5]. The test matrix required nine devices from each manufacturer. During testing some Micron devices failed functionally, requiring use of three backup devices to fill out the test matrix. The test devices used are summarized in **Table 2-1**. A photo showing three Samsung devices is shown in **Figure 2-1**.

Table 2-1. Devices used for stress testing.

Manufacturer	Part Number	Feature Size	Memory Size	Stress	# Parts
Samsung	K4T2G084QA-HCF7	78 nm	2 Gb	2.7 V 125ºC	3
Samsung	K4T2G084QA-HCF7	78 nm	2 Gb	1.8 V 125ºC	3
Samsung	K4T2G084QA-HCF7	78 nm	2 Gb	2.7 V 25ºC	3
Micron	MT47H256M8HG-3:A	78 nm	2 Gb	2.7 V 125ºC	TBD
Micron	MT47H256M8HG-3:A	78 nm	2 Gb	1.8 V 125ºC	TBD
Micron	MT47H256M8HG-3:A	78 nm	2 Gb	2.7 V 25ºC	TBD

Figure 2-1. Samsung DUTs mounted to DUT boards.

2.3 DIMMs as Future Test Vehicle

During collaborative discussions this year we determined that many test groups have moved toward use of automated test equipment designed to test DIMMs as their hardware of choice for DDR2 testing. Although we think this approach is somewhat narrower in scope than needed for this task, we believe DIMMs may be a viable alternative for characterizing devices.

One key way that DIMMs can enable the type of testing desired under this task is by reducing effort and cost involved in obtaining test devices. Once we included all of the part preparation costs (including DUT board and mounting) we determined that each DUT costs approximately $150 to prepare for life testing. For future testing we wish to test at least 50, and possibly as many as 100 DUTs. The price tag associated with this quantity of DUTs is reduced if they are mounted on DIMMs. For 2-Gb DDR2 devices mounted on a DIMM (thus, a 2-GB DDR2 DIMM with eight devices), the cost is approximately $50 per eight devices, or $12.50 per DUT. Thus, for 100 DUTs we can expect a cost savings of more than $13k. Additionally, the DUTs can be procured directly from a very large number of sources. The only significant problem with this approach is that DIMMs are not manufactured as a vehicle for technology testing, and as such we will have difficulty locating more than eight DUTs with similar lot/date codes at a time.

3.0 TEST SYSTEM AND DEVELOPMENT

During FY11, development continued on the DDR2 Reliability Tester (D2RT). Development included demonstrating simultaneous operation of nine of the D2RT units, controlled by three computers. Development also included functional verification of the alternate 8-DUT Mezzanine Card B (MCB) which enables a single D2RT unit to test eight DUTs simultaneously.

In addition to improvements to the existing hardware envisioned for the D2RT, we also carried out two other hardware development studies. The first is establishing the need for the D2RT to be able to operate industry-standard DIMM units to reduce general DUT costs when sample size and breadth is a larger concern. And the second is that we researched ways to utilize the JPL Radiation Effects Group's Eureka2 DDR/DDR2 test system.

3.1 Test System

The D2RT test system was originally developed for the 2010 NEPP Scaled CMOS Reliability task. It is designed as a generic FPGA-based system that uses a standard Xilinx Virtex 4 development board and an Opal Kelly USB interface board.

3.1.1 General Structure

The test system is composed of the hardware structure (motherboards, mezzanine boards, DUTs, DUT boards, Opal Kelly communication unit, and operations laptops), the firmware developed to control the actual D2RT test units, the firmware developed to control the Opal Kelly USB2 connection, the firmware to control the Opal Kelly to D2RT connection, and the software to interface the firmware to the test engineer.

An individual D2RT test unit with connection all the way from the DUT to the data collection computer is shown in **Figure 1-1**, while the test head of the system is shown in a photo in **Figure 3-1**. The computer is controlled with software designed to interface with the Opal Kelly USB interface to provide interaction with the firmware on the FPGA eval board. This connection is accomplished by communicating through a standard wire in/wire out/pipe in/pipe out interface on the Opal Kelly into a custom IO interface called IO16 which is implemented between the Opal Kelly and the FPGA eval board. On the FPGA eval board, a register file-based firmware structure is employed to provide a standard and symmetric interface between the test software and all write and read values in the D2RT test system. After the register file, individual demons or port control units are custom-built for the specific test application desired. A generic high-speed (125 MHz clock) DUT operation unit was used for DUT operations this year.

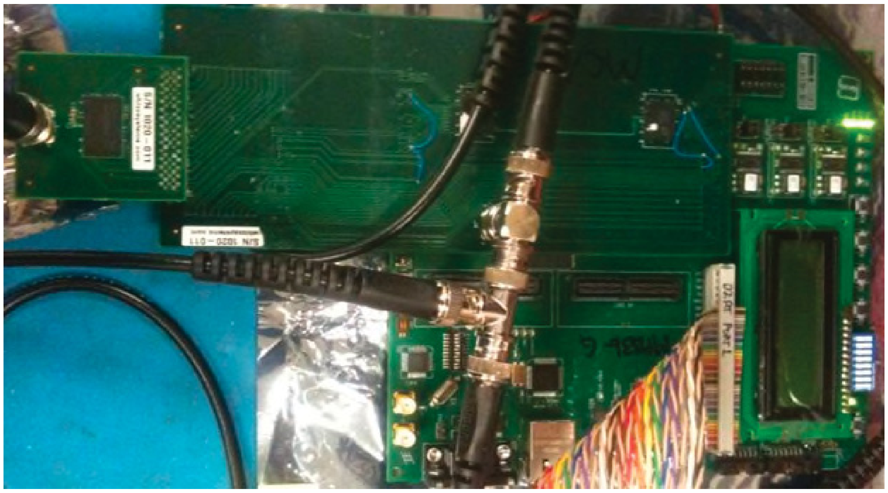

Figure 3-1. Complete motherboard, mezzanine card, and DUT with IO16 connection and power connections.

The hardware architecture for the full 9-DUT test system with environmental chambers is symmetric among identical hardware elements. The hardware layout is shown in Figure 3-2.

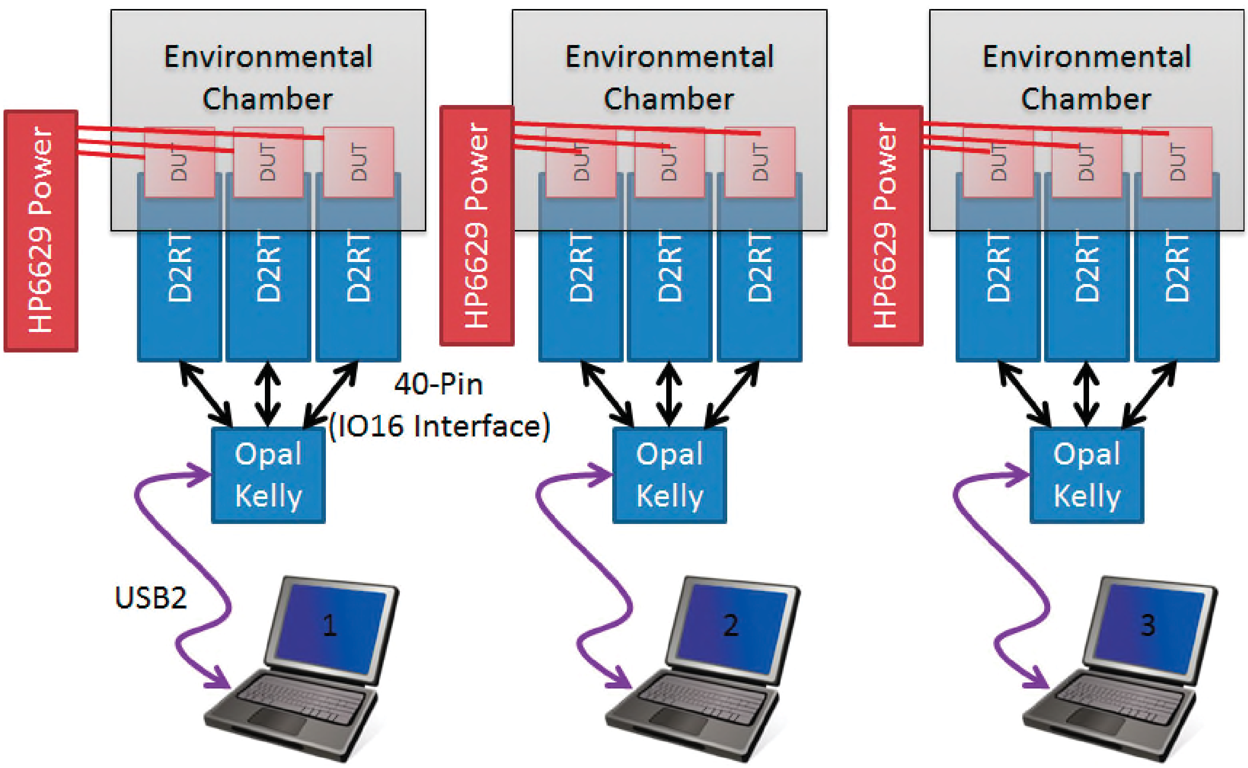

Figure 3-2. Hardware layout for the D2RT reliability test system with nine DUTs.

3.1.2 Developed Equipment

The 3-DUT test system developed for FY10's early testing is pictured in **Figure 3-3**. This system was expanded to support three simultaneous computer systems operating three DUTs each.

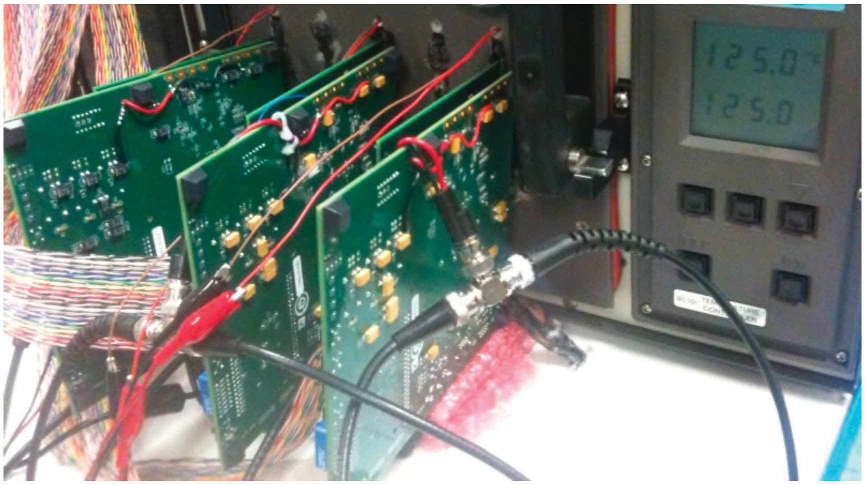

Figure 3-3. The 3-DUT test system is shown with MCA cards inserted into the environmental chamber.

3.1.3 System Performance

The tester achieved the following benchmarks:

1. DUT Clock Speed: 125 MHz
2. DUT Average Data Rate: 2×10^7bits/second
3. Temperature range: 25ºC to 125ºC
4. Voltage range: 1.7 V to 2.7 V
5. DUTs per D2RT system: one
6. Maximum simultaneous D2RT systems: nine
7. Refresh rate: 371 ms

3.1.4 Limitations

The single largest problem with the test system this year was that it required too much maintenance to operate correctly, and as a result it was expensive and some of the data became compromised. Given the desire to test up to 48 or more devices simultaneously, this problem must be addressed in the future. Automation of test software to enable the engineer to know that things are working correctly, and automatic operating of power supplies within the test software would be the simplest and most effective software updates.

A significant additional benefit comes from removal of operation outside of the part's required SSTL-18, which requires reprogramming the D2RT with different firmware between 2.7 V stress and 1.8 V nominal health monitoring.

FY11 testing utilized a non-standard method for device refresh that requires manually refreshing the DRAM cells. For this method to work, a specific addressing scheme is required to achieve the fastest possible refresh rate achievable with the test system. During testing this year we determined (by data analysis) that the maximum effective refresh rate (designed to be 11 ms) was 371 ms. We have since developed firmware updates that enable the device to be refreshed significantly faster than 11 ms.

The last point to mention regarding limitations was that the life-test approach for determining DUT health simply was not very useful. This is demonstrated in the test data. More discussion on the approach and methods to improve it in the future can be found in Section 5.0.

3.2 8-DUT Mezzanine Card

The 8-DUT mezzanine card known as Mezzanine Card B (MCB) was developed during this fiscal year to enable individual DUT ports to be accessed by changing firmware on the motherboard. This system was verified to provide signals to all ports; however, we did not develop a multi-DUT setup capable of operating all the DUTs without a firmware reload. The testing this year validated the hardware design and capability of the MCB to operate in its desired capacity. In order to utilize this, however, a significant number (>30) additional loose DUTs would be required.

3.3 Collaboration on DIMM Adapter

Discussions with Ray Ladbury of GSFC highlighted the potential benefit of interchangeable test systems between JPL and GSFC. Since GSFC is using industrial automated test equipment (ATE) to perform testing of DIMM units, we decided it would be worthwhile to investigate the potential of the D2RT to support DIMM operation.

Initial studies indicate that unbuffered DDR2 DIMMs present a straightforward interface to connect to the Xilinx Virtex 4 FPGA on the D2RT. We also verified that existing board reference designs existed to aid board layout and fabrication needs. A new mezzanine card (MCC) will be developed in FY12 to take advantage of DIMM test devices. More information on the potential benefits of DIMMs can be found in Section 2.3.

3.4 Use of the Eureka2

During FY11, the JPL Radiation Effects Group obtained a Eureka2 DDR2 test system. This tester is designed to test DDR and DDR2 devices for acceptance testing, but can also be modified by request to Eureka to modify the firmware or software in order to enable testing specific parameters. A picture of the Eureka2 tester is shown in **Figure 3-4**.

Special adapter boards were made to support running the DDR2 test devices, designed to connect to the MCA, into the Eureka2 test system. Although this appears to be a viable way to run the DDR2 test devices we obtained for the FY11 testing, future test parts will likely target the DIMM approach, and the Eureka2 will be used as a DIMM tester (as designed). The custom adapters are pictured in **Figure 3-5**.

Figure 3-4. The Eureka2 test system [6].

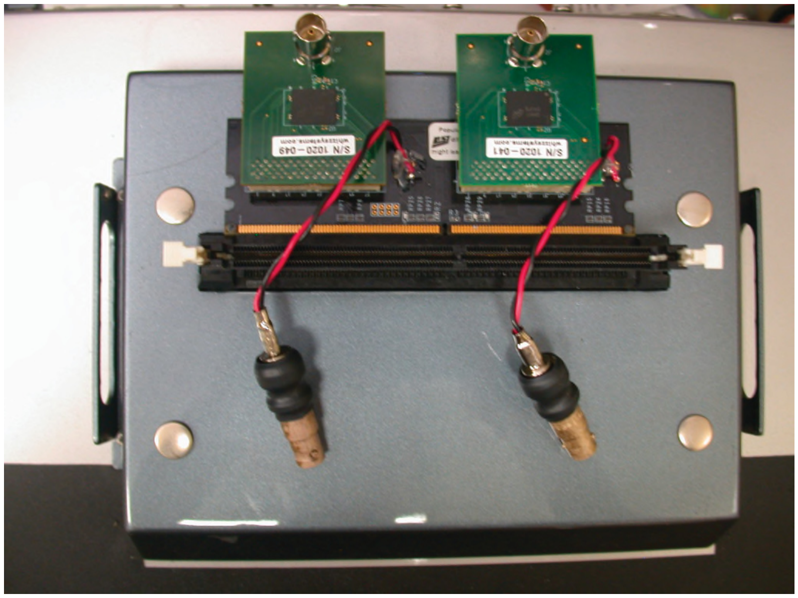

Figure 3-5. Eureka2 to JPL DUT adapter.

4.0 TESTING

Micron and Samsung 78-nm, 2-Gb DDR2 SDRAMs were tested using voltage and temperature acceleration in order to explore reliability and degradation mechanisms. Testing was performed on three sets of three devices, for a total of nine devices each, from Samsung and Micron. Test conditions were chosen to be similar to those in previous testing of DDR devices [2]. In particular, we chose to employ 1.5 times the nominal voltage and a temperature of 125°C. These values are not included in the device operational specification; therefore, we did not expect the devices to work correctly during stress testing. However, periodic health checks were performed under nominal operating conditions to evaluate the status of DUTs during the life test exposure.

This work shows that under a constant test pattern and nominal operating conditions, most of the devices showed little degradation of storage cells. However, some Micron devices were found to show early signs of elevated operating current, and some devices failed. Failures are apparently due to elevated operating voltage (2.7 V stress on a 1.8 V rated part). However, the sample size was too small to establish statistical relevance of this stress on the devices because there was no significant observed degradation before failure. The Samsung devices were not observed to fail as a result of this voltage stress.

4.1 Test Plan

Life testing was performed on Samsung and Micron 2-Gb DDR2 devices. The primary goal was to examine voltage and temperature acceleration. As such, the final test matrix for these factors is shown for Samsung in **Figure 4-1**, and Micron in **Figure 4-2**. We targeted a temperature range of -25°C to 125°C, and 1.8 to 2.7 V. Because of lack of observed temperature acceleration, we narrowed the test range to between 25°C and 125°C, and the lower temperature area (-25°C) was not examined.

Testing was designed for comparison to the work performed for the 2010 Scaled CMOS NEPP task [1]. To achieve comparable data sets, we monitored the data retention of the 1-transistor, 1-capacitor DRAM cells in the devices under stress conditions similar to those used in [1].

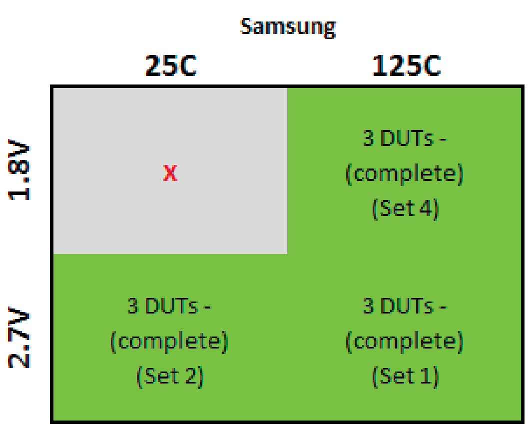

Figure 4-1. Samsung test matrix.

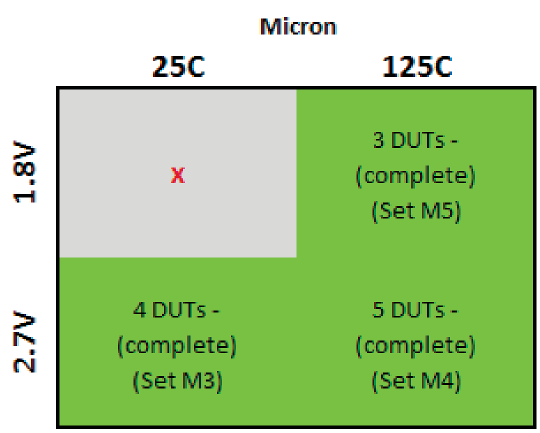

Figure 4-2. Micron test matrix.

Testing followed an algorithm intended to provide stress while also enabling periodic monitoring of device health. The algorithm used is as follows.

1. Device is tested for data retention at 25 and 85°C
2. Device is prepared for operation at elevated voltage and/or temperature
3. Device is operated under stress for 250 hours
4. Device is returned to nominal conditions and tested for data retention at 25 and 85°C
5. Steps 2 to 4 are repeated until the desired stress duration is achieved.

Note that step 3 is performed by resetting the running test system approximately once per 48–72 hours. Thus we have measurements of current draw by test devices between the 250-hour data retention measurements.

4.2 Test Operations

The tests on the DDR2 parts consist of pre-, post-, and periodic characterization between periods of stressing the parts by stimulating them with continuous read/write operations at either 1.8 V or 2.7 V while the temperature is held at a constant value (25°C, or 125°C). The setup to achieve these levels is described in Section 3.1.

4.2.1 Nominal Voltage Setup

Characterization of the DUTs between periods of stress is performed at the nominal voltage value of 1.8 V. To run at this level, it is important that the FPGA is programmed using the firmware version specified for this voltage. After programming the FPGA, the voltage levels for the FPGA IO ports can be run at 1.8 V. With the FPGA properly configured, the test system mezzanine board and the DUT card are then set to 1.8 V.

4.2.2 Nominal Temperature Setup

Nominal temperature for this testing is defined as room temperature. Application of room temperature was provided by either building air conditioning, or by the nominal temperature achieved inside the thermal chambers with no thermal control (i.e., they were in equilibrium with the environment in the room). During the testing room temperature fluctuated due to the building air conditioning and due to some measurements being made inside and others outside a thermal chamber. It is estimated that the range of values designated “room temperature” range from 22°C to 30°C. This difference is large enough to cause significant variation (up to 10 times as many failed bits) in the 25°C measurements.

4.2.3 Voltage Stress Setup

To induce voltage stress, the parts are run at 2.7 V. In order to achieve 2.7 V (1.5 × Vdd) operation, the test system configures the DUTs with 2.5 V Stub Series Terminated Logic (SSTL) compatible signals, then runs at the high side of the specification [7], delivering 2.7 V. To do this, the FPGA needs to be programmed with the firmware version that is specified for 2.7 V. After it has been programmed, the DUT and mezzanine card can ramp up their voltage, in parallel, to 2.7 V.

Unfortunately, it is not specified what the DUT does when exposed to 2.7 V. In particular, we believe that protection diodes will kick in by this level. Even poor protection will hold at 0.7 V above nominal, and we were running 0.9 V above. This results in a complex test case because the internal regulation may be very strongly held to 1.8 V, rendering it impossible to achieve the desired voltage acceleration. Furthermore, any internal regulation will also modify the switching levels for the IOs in both directions. These issues result in unknown signals being driven onto the DUT and non-sensible signals being driven by the DUT.

4.2.4 Temperature Stress Setup

Tests performed at temperatures other than room temperature, such as specification maximum (85°C) and thermal stress levels (125°C) are performed with the DUT running inside a thermal chamber. The mezzanine board runs through a chamber door with its DUT card connection inside the chamber to expose the DUT to the temperature environments. On the other side of the mezzanine board, the FPGA, USB interface card, and computer are all external and operating at room temperature. The chamber and modified door are capable of accommodating three mezzanine boards and simultaneously exercising three DUTs. The 25°C, or room temperature, test uses the same electrical interfaces, but the mezzanine board is not necessarily used as a physical bridge into an environmental chamber.

4.2.5 DUT Operation under Stress

In order to examine reliability mechanisms in the cells of the DDR2 devices, it is necessary to apply stress fields within the data storage elements. This is the reason the DUTs must be operated during stress exposure. By operating the DUTs in a refresh mode during elevated voltage and temperature exposure, the DUT cells will hold higher internal electric fields, which are required for activating some failure mechanisms.

The DUTs are fully operated under stress, by performing read and write operations that also refresh the data as a byproduct (originally designed to refresh faster than once every 32 ms; following data analysis, it was determined the refresh rate is closer to 400ms). The entire DUT address space is sampled. The pattern used to program the cells is address-based, ensuring exactly 50 percent of the bits are '0's and 50 percent are '1's. By performing these operations on the DUT under stress, we ensure that pattern dependence is sampled roughly, and that the entire device must be working in order to get the test setup to pass requirements for data taking.

Stress testing calls for 2.7 V operation of DUTs. This is out of specification, and thus the operation of the DUT cannot be tested in a normal way at this voltage. It was inferred that DUT operation was nominal during elevated voltage stress by the following observations. The currents changed in similar ways at 2.7 V during operation as they did at 1.8 V during operation. Many of the bit lines actually operate nominally at 2.7 V. (This is not at all predictable, because the Vref is completely out of specification, and the DUT is expected to be internally regulating power, this means the detection of logic high and logic low may be significantly altered.) Finally, the 2.7 V operation is considered nominal if it is also shown that upon returning to 1.8 Volts the DUT operation returns to (potentially degraded) earlier observed operating conditions.

4.3 Results

Test results were collected for all test matrix points. This section briefly provides highlights of the test results. The full report on all results of this testing can be found in [3]. In particular, the following measurements are available for all DUTs in [3]:

1. I_{DD3N} for each DUT as a function of stress from pre-stress to post-stress at all characterization points
2. I_{DD4R} for each DUT as a function of stress from pre-stress to post-stress at all characterization points
3. I_{DD4W} for each DUT as a function of stress from pre-stress to post-stress at all characterization points
4. Cell retention curves measured between 370 ms and 2 hours for room temperature at all characterization points

5. Cell retention curves measured between 370 ms and 2 hours for elevated temperature (usually 85°C) at all characterization points
6. Details about DUT failures during testing.

4.3.1 Samsung

The Samsung devices showed minor changes in operating currents for the worst case test lot (2.7 V, 125°C). This change was only about 5 mA after 1000 hours of life testing for I_{DD3N}, I_{DD4R}, and I_{DD4W}. The plot of this performance is shown in **Figure 4-3**.

No significant changes in retention curves were observed. In **Figure 4-4** below we see a typical device cell retention curve, in this case taken from the Samsung DUT set exposed to 2.7 V and 125°C. Note that for some of the test devices, initial characterization at 75°C was modified so that characterization (not the life test stress) was performed at 85°C. This figure also provides evidence of minor changes at 25°C, however this temperature was regulated by room air conditioning and the error in the actual temperature easily accounts for the difference in the data points.

4.3.2 Micron

Micron devices showed no significant parametric shifts in operating current and cell retention. This holds for all test points. The only significant comment related to the results of Micron testing is that three devices failed to function as a result of the stress environment. Two devices failed during 125°C/2.7 V testing, and the third failed during 125°C/1.8 V testing.

Figure 4-5 shows typical I_{DD4W} operating current for Micron devices life tested with 125°C/2.7 V. This figure shows essentially no change in operating current on any of the test devices for the duration of the exposure.

Additional typical data is shown in **Figure 4-6**. This example shows two behaviors seen in all test parts. The first is the skew in the data at 25°C, which is due to limited thermal control of the test condition in the laboratory and likely shows a difference of about 3–5°C between measurements. The second is that minor imprinting appears to have occurred and is evidenced by the slightly improved post-stress retention curve, indicating the cells can hold data longer after stress. Note that the data pattern during stress is constant and the cell retention is measured with the same pattern.

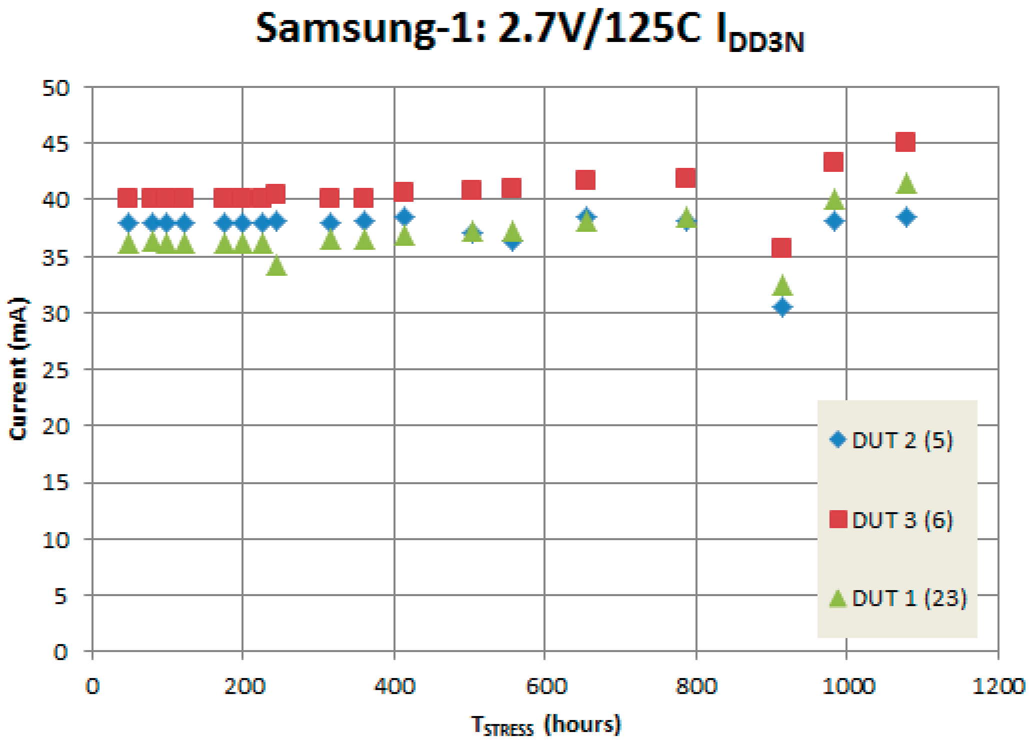

Figure 4-3. I_{DD3N} for the worst-case change in Samsung test lots.

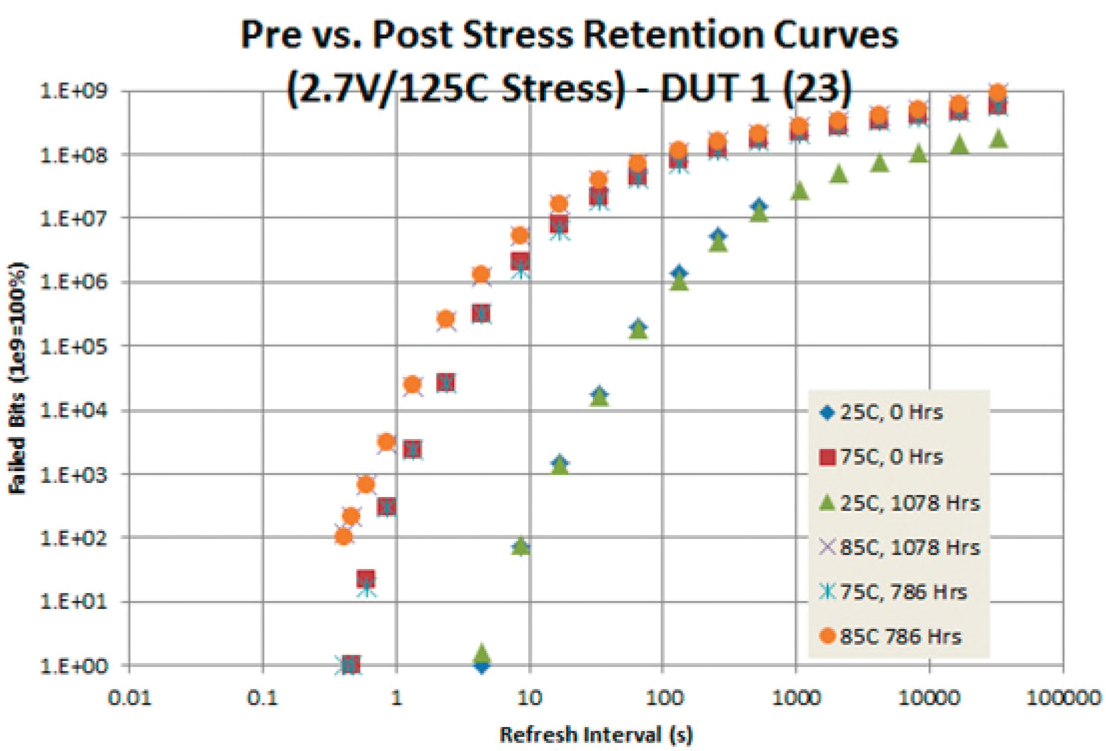

Figure 4-4. Typical retention curve for a Samsung device before and after life test exposure.

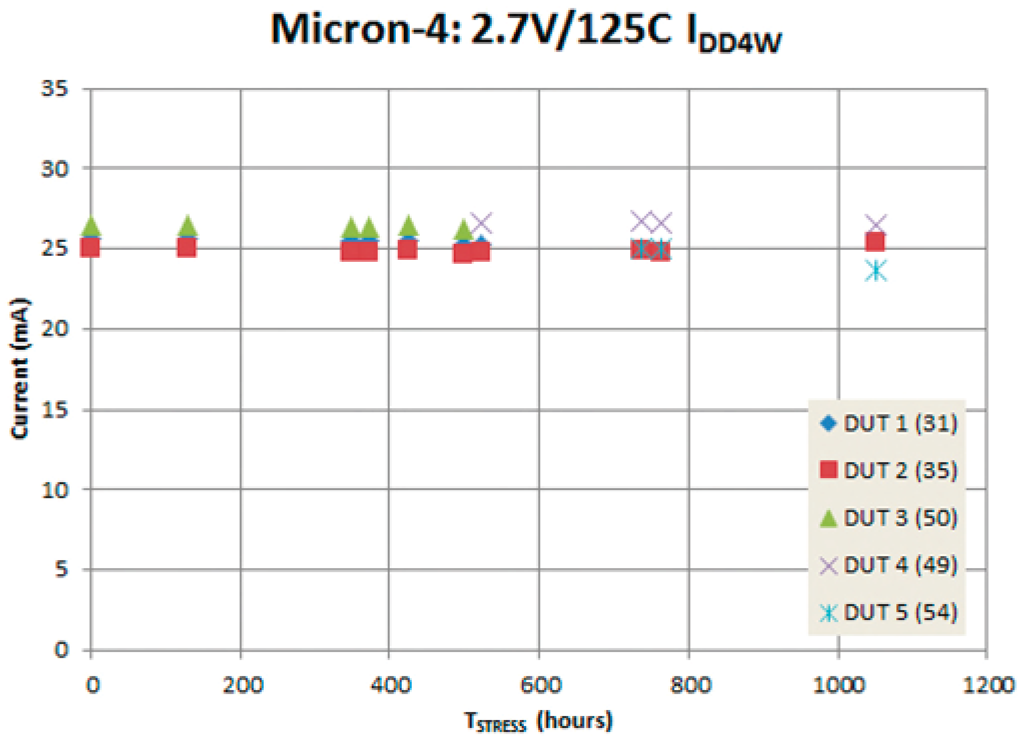

Figure 4-5. Sample development of I_{DD4W} for Micron DUTs exposed to 125ºC/2.7 V.

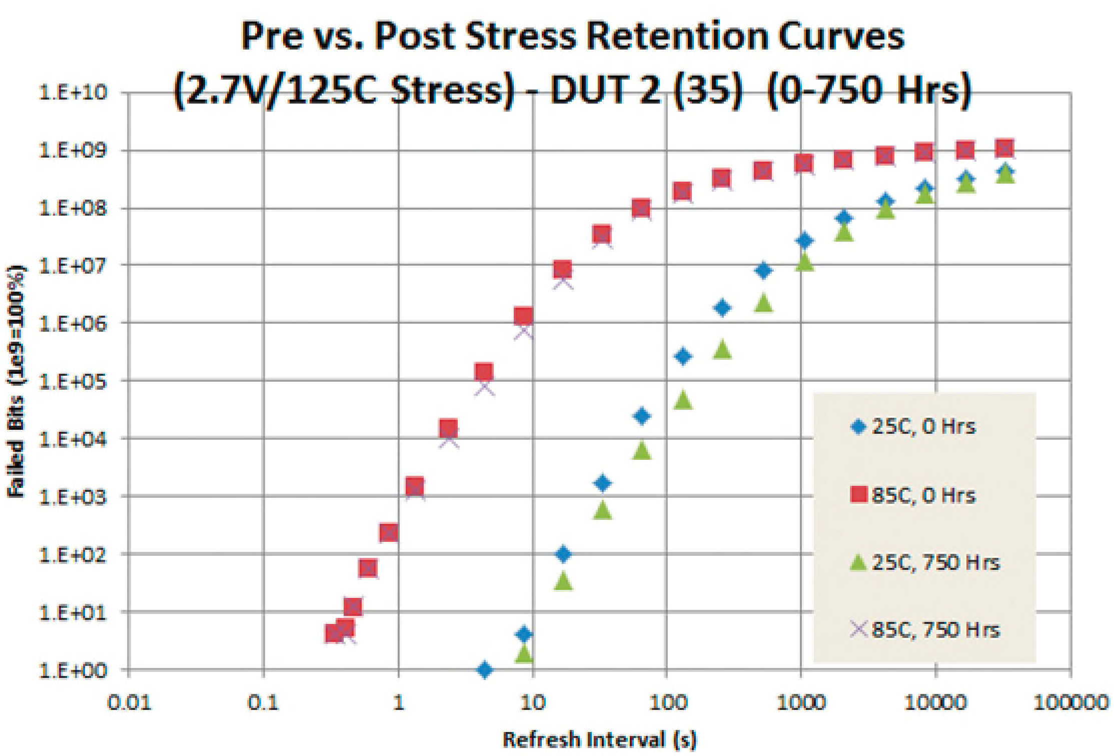

Figure 4-6. Sample of pre- vs. post-stress cell retention for a DUT exposed to 125°C/2.7 V showing only minimal change except for minor imprinting at 85°C and skewing due to limited thermal control at 25°C.

4.3.3 Summary of Results

This year's life testing showed limited changes in the DUTs during life stress testing. This result spans all test matrix points (125°C/2.7 V, 125°C/1.8 V, and 25°C/2.7 V) on both manufacturers (Samsung K4T2G084QA-HCF7 and Micron MT47H256M8HG-3:A). We believe that the key cause of this result is on-chip voltage regulation (however other explanations are possible). Furthermore, the number of test samples is limited compared to the goals of reliability testing as a general practice. With the lack of observable change it is not possible to draw conclusions about what parameters may fail in a small subset of parts.

Only minor changes were observed. Some high-temperature operating currents trended gradually higher. In addition, some data imprinting may have been observed, but it is of a statistical nature and not believed to be applicable at the bit level. Three Micron devices failed during elevated temperature testing (two at 2.7 V, and one at 1.8 V); however, it is believed these failures relate to operating circuits and not the storage cells.

The primary goal of this work is to identify the leading failure indicators of this technology. The idea is to observe cell degradation since it is expected to show observable variation as a result of the stress. However, since this was not observed, we must conclude that either other parameters are more important or that insufficient data was collected and/or stress duration was inadequate.

This testing indicated that the following changes should be made to future testing. First, different patterns should be used to sensitize the DUTs and verify functionality. Second, voltage stress should not exceed the manufacturer's maximum voltage rating because protection circuits are likely to be present and the system cannot reliably operate the DUT. (This is exaggerated by the fact that there are no datasheet parameters to guide operational parameters, and that the test system is not running a defined IO protocol during elevated voltage testing unless it switches from SSTL-18 to SSTL-2; i.e., it cannot be gradually scanned to determine a good stress voltage). Third, thermal stress should be used as a varying parameter to determine the likely level of failure (i.e., maximum temperature where the circuit still works)—this is especially important because periodic refresh must work properly to bias the test cells. Fourth, the DUTs should be exercised using a more standard refresh method that ensures the cells are refreshed every 32 or 16 ms. Fifth, a larger sample size is required—this limits the need to swap in parts as a result of failure and increases the significance of results and likelihood of finding outliers; a minimum of 10 DUTs per test point is suggested.

5.0 TEST APPROACH REVIEW

During this fiscal year it became apparent that the primary test approach, which was originally targeted at determining the breakdown mechanisms for technology, needs to be redirected toward the most relevant reliability issues for packaged DDR2 devices of interest to NASA. To address this issue several fronts were examined. First, the spectrum of data sheet specifications which might make up a useful test matrix to analyze devices for reliability issues must be reviewed. Second, NASA users of DDR2 have much more time than the manufacturer to perform initial characterization testing on a per device basis and NEPP can help establish test methods to identify the best devices to be used in applications. And finally, NASA users may intentionally want or need to operate devices off of the datasheet, and this task can help users identify which devices will perform sufficiently well in these cases.

5.1 Datasheet Parametric Review

Due to limited impact of the approach for reliability characterization of DUTs during FY11, critical review of the parametric measurements performed on the DUTs was performed. Initial efforts focused on the datasheet parameters until this was determined to include too many parameters to be viable.

Datasheet parameters listed for the Micron 2Gb DDR2 include the following:

- Five sets of standard DC-level voltage limits
- Three sets of standard DC-level leakage current limits
- Two sets of thermal limits
- Five CAS Latency Settings
- Seven Write Recovery settings
- 15 general timing limits
- 14 operating currents
- 11 clock and strobe eye-diagram parameters
- 21 DQS timing requirements
- 21 command and address timing requirements
- 21 additional timing requirements
- Five operating voltage requirements (stricter than limits)
- Three Driver strength curves.

Many of the parameters listed above increase the test matrix multiplicatively by providing alternate test modes in which all of the other parameters should be tested under each such mode.

Because of the expected lack of reliability sensitivity to many of the test situations suggested by the above list, it is likely unnecessary to test a very many unique scenarios. Careful examination of the general concept behind each parameter type can indicate specific test cases that cover the limiting cases. Analysis of the requirements suggests the test list indicated in **Table 5-1**. This table specifically does not address I/O capacitance or standard input timing parameters other than frequency. In the latter case, we believe that no significant parameter is likely to degrade more than the read and write latencies that are already tested (in a limited sense due to the maximum tester clock of 125 MHz). (The reason is that these tests will show circuit degradation from both signal propagation and cell access and we are not concerned which of these two is the cause of any degradation as long as degradation is observed.)

Note that the operating currents are taken for each test. Standby current refers to whatever the low-power mode is used (for example, declocked). Refresh current refers to the current during any refresh-only operation (even if it is below the specification refresh rate—for example at 0°C the refresh required to hold data is expected to be longer than 1 s).

Table 5-1. Recommended test types to meet the general concept of most data sheet parameters.

Test	Target Parameter	Type	Tester	Result
Frequency Sweep	Operating Frequency Range w/out DLL	Shmoo	D2RT	Range
Frequency Sweep	Operating Frequency Range with DLL	Shmoo	Eureka	Range
Voltage Sweep	Operating Voltage Range	Shmoo	D2RT	Range
Output Levels	Voh, Vol	Waveform	Scope/Eureka	Pass/Fail
Input Levels	Vih, Vil	Signal Level	Eureka	Range
Cell Retention @0ºC	Low Temperature Retention (3+ patterns)	Retention Curves	D2RT	Curves
Cell Retention @85ºC	High Temperature Retention (3+ patterns)	Retention Curves	D2RT	Curves
Temperature Limits	Correct operation (possible data loss)	Shmoo	D2RT	Range
Minimum Refresh @0 ºC	Refresh rate required to retain all data for at least 1 hour	Limit	D2RT	Min. Rate
Write Delay	WL+/-t_DQSS	Shmoo	Credence	Range
Read Delay	RL+t_LZ{min,max}	Limit	Scope	Pass/Fail
Operating Currents	Standby, Refresh, Read, and Write	Measurement	Any	Pass/Fail

5.2 Initial Characterization Testing

Initial characterization of DUTs plays directly into the period health checks that will be performed. Thus, any measurement we may want to make on the DUTs must initially be performed before stress is carried out. The largest benefit gained by initial characterization testing is to identify parameters that may help to eliminate early failures in a similar way that a program could do prior to building circuits.

Based on **Table 5-1**, we see that there are actually quite a few test types that can be run initially. Note that some tests may be destructive and can be run on sibling devices to establish the range at which devices work.

One example is the voltage range for operation, which may unnecessarily stress test devices that will not get voltage stress. This may not be entirely true, because after a high-voltage exposure where the DUT does not work properly, the DUT may still be fully functional and the lack of operation could be due to limitations on the voltage range where the device works correctly due to protection circuits.

5.3 Off-Datasheet Operation

The discussion in Section 5.1 alluded to operating the DUTs off the datasheet. There are two reasons identified where projects may want to do this. They both occur because the datasheet is intended to provide corner cases where the device will function properly and because the datasheet does not document all operating modes of the devices. The two off-datasheet operations discussed here are low operating frequency and low device refresh rate.

Low operating frequency is supported on devices in a “test configuration” to enable operation without requiring a DLL lock. Although the datasheets indicate no maximum, it is expected that devices will function up to 66 MHz without a DLL lock. This is very slow compared to the design case for these devices, but it may be desirable for circuits to operate this way in some applications.

Low refresh rate operation is part of a low-current option for device use. The device refresh is used to ensure that the storage cell voltages are kept at levels that clearly indicate the stored values. The cells lose this voltage much more quickly at high temperatures such as 85°C. Because the datasheet provides the corner case of the refresh rate that will work across all temperatures, it is necessarily much higher than would be required for 0°C operation. Because the self-refresh current with CKE low is only about 10 mA, which is low compared to nominal, it may be the case that devices continue to use a similar level of power even when the refresh rate is very slow.

5.4 Data Pattern Sensitivity

Data pattern sensitivity is an example of a measurement that this NEPP task can make in-depth. For future characterization, data pattern sensitivity can be examined against the following:

1. Device Intrinsic Pattern (Bleed Down)
2. Inverse Bleed Down Pattern
3. Checkerboard
4. Inverse Checkerboard
5. Pseudo-Random A
6. Pseudo-Random B (different seed than A).

These patterns should all be tested for variations in cell storage capability.

In addition to cell-storage patterns, disturb-based operations can be used such as March X or walking 1's/0's.

6.0 FUTURE WORK

In FY11 some key information was developed which can be used to improve work in FY12 and beyond.

6.1 Establish Updated Parametric and Device Health Monitoring Approach

In FY11, it was determined that the three primary parametric measurements taken as part of the evaluation of device health during periodic characterization were insufficient. Future test planning will include an expanded set of parametric measurements including: alternate device timing, pattern dependent data retention, off datasheet operation, and expanded fundamental device parameters.

6.2 Future Testing

For FY12 we will develop a test approach to enable the following:

- We will determine an initial sampling approach for evaluating DUTs for quality and reliability.
- We will perform initial sampling of initial device quality for 48 to 64 devices, based on availability of DIMM modules.
- If an appropriate life test can be established based on initial sampling results, 16 to 24 DUTs will be exposed to life testing and repeated sampling of device quality.

6.3 Update Hardware for Test System

For FY12, the primary hardware update desired is to develop a DIMM adapter for the D2RT. This will eight or more DUTs per D2RT motherboard.

6.4 Update Firmware for Test System

FY11 firmware has been reviewed and modifications are required to perform the following:

1. Reduce refresh rate to 11ms or faster
2. Enable alternate test patterns – fixed value, fixed value alternating, and random
3. Increase data throughput by 2×
4. Enable testing at 33 MHz clock (as an option of potential relevance) (in addition to 125MHz)
5. Enable testing of DIMMs under new hardware.

6.5 Update Software for Test System

The test software used to run D2RT motherboards was not user-friendly. This led to data files that were very difficult to analyze, complicated user operations, and in some cases compromised data. These problems will be addressed to improve test results for FY12.

7.0 SUMMARY

Test efforts for DDR2 devices for FY11 provided the following summary findings. Life testing this year did not show significant degradation, indicating that either the test conditions were not likely to lead to failures or the characterized parameters were insufficient to detect reduced performance. Device life testing must be performed within the limits of the datasheet. Parametric characterization must focus on general operation and cell performance tests that are time-intensive, because manufacturers are unable to perform long duration device characterization on every device, but such characterization be performed for NASA missions.

Life testing was performed in FY11 on Samsung and Micron 78-nm DDR2 devices. DDR2 devices cannot be reliably tested to determine technology reliability by means of temperature or voltage acceleration beyond the datasheet specifications. The findings this year indicate that there was no functional change and no significant parametric degradation of performance up to 1000 hours of life testing under stress, except for the case of Micron devices where 3 out of 12 total test devices digitally transitioned from working to failed at various times during stress testing. This is believed to be due to elevated operating voltage. This finding does indicate possible reliability impact worth studying but does not provide information on the technology of the cells, which was the primary goal of the FY11 testing. The only technology finding is that it appears that some DUTs seemed to retain the test pattern (which was constant for the full 1000 hours) better after storing it under the stress conditions (i.e., the part was able to retain data longer without refresh).

Micron devices failed functionally during this testing, but with no warning beforehand. Lack of degradation before failure may not be something that can be improved; however, the test protocol can be improved to ensure reliable handling of devices, limited mechanical work, and elimination or careful examination of any use outside device specification.

We analyzed methods to improve parametric testing used to establish device operation characteristics during stress testing. The findings of this effort indicated that the sheer number of potential parametric measurements is beyond the scope of this task, but a carefully selected subset can expose reliability concerns that may not have been identified by the manufacturer. Individual parts may have operation problems that cannot be quickly identified and due to volume cannot be caught by the manufacturer. Reliability test efforts must focus on observing pre-stress characterization, identifying substandard initial operation, and linking abnormal initial observations with those devices at higher risk for problems during life testing.

For the future, primary work needs to focus on the expansion of device characterization, improved acquisition of test devices, and expanded test capacity targeting DDR2 DIMMs and DDR3 options.

8.0 REFERENCES

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APPENDIX A. ACRONYMS AND ABBREVIATIONS

ADC	address, data, and control
CMOS	complementary metal oxide semiconductor
DDD	displacement damage dose
DQ	data line where Q is 0-7
DUT	device under test
FBGA	fine ball grid array
FPGA	field programmable gate array
FSM	finite-state machine
GSFC	Goddard Space Flight Center
IDD	total device current
IDD(q)	Idd drawn by device while in operating mode q.
I/O	input/output
JPL	Jet Propulsion Laboratory
LCDT	low-cost digital tester
MCB	mezzanine card B
MCA	mezzanine card A
NEPP	NASA Electronic Parts and Packaging
SSTL	Stub Series Terminated Logic
TID	total ionizing dose
TBC	to be confirmed
TBD	to be determined